## Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

## Listing of Claims:

1. (Currently Amended) A method for fabricating a non-volatile memory device, the method comprising:

providing a silicon substrate;

forming an oxide layer <u>overlying on</u> the <u>silicon</u> substrate, the oxide layer having an amorphous surface structure;

forming a buffer layer on the amorphous oxide layer after forming the oxide layer over the substrate, the buffer layer having a crystalline structure;

thermally annealing the buffer layer to enhance an alignment of crystallites of the buffer layer;

forming a ferroelectric material overlying the substrate and on the buffer layer;
forming a gate layer overlying the ferroelectric material, the gate layer overlying a channel region; and

forming a first source/drain region adjacent to a first side of the channel region and a second source/drain region adjacent to a second side of the channel region.

- 2. (Original) The method of claim 1 wherein the channel region is about 1 micron and less.
- 3. (Original) The method of claim 1 wherein the ferroelectric material is a PZT bearing compound.
- 4. (Original) The method of claim 1 wherein the buffer layer is a magnesium bearing compound.
- 5. (Original) The method of claim 1 wherein the buffer layer is a magnesium oxide layer, the magnesium oxide layer being a barrier layer.
- 6. (Original) The method of claim 1 wherein the ferroelectric material has a thickness of less than about 1,000 Angstroms.

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- 7. (Original) The method of claim 1 wherein the buffer layer has a thickness ranging from about 7 to 100 nanometers.
- 8. (Original) The method of claim 1 wherein the ferroelectric material has a thickness of about 100 Angstroms and greater.
- 9. (Original) The method of claim 1 wherein the ferroelectric material is PZT.
- 10. (Original) The method of claim 1 wherein the buffer layer is a barrier diffusion layer, the barrier diffusion layer substantially preventing diffusion between the ferroelectric material to the substrate.
- 11. (Original) The method of claim 1 wherein the buffer material is sputtered from a substantially pure magnesium target to form a magnesium oxide layer.
- 12. (Original) The method of claim 11 wherein the sputtering is maintained at a temperature greater than about 400 degrees Celsius or greater than about 500 degrees Celsius.
- 13. (Previously Presented) The method of claim 11 wherein the buffer layer is thermally annealed at a temperature of 800-1000 degrees Celsius for about 30 minutes.
- 14. (Original) The method of claim 1 wherein the ferroelectric material is highly oriented.
- 15. (Original) The method of claim 14 wherein the highly oriented material is a polycrystalline film.
- 16. (Previously Presented) The method of claim 1 wherein the ferroelectric material is substantially free from an amorphous structure.
- 17. (Original) The method of claim 15 wherein the polycrystalline film has a crystal structure of 100 angstroms and greater.
- 18. (Previously Presented) The method of claim 1 wherein the buffer layer is a template to provide an oriented growth of the ferroelectric material.
- 19. (Previously Presented) The method of claim 1 wherein the oxide layer is provided by a dry oxidation process comprising an oxygen bearing compound.
- 20. (Previously Presented) The method of claim 1 wherein the oxide layer passivates the surface of the substrate to protect the channel region.

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21. (Currently Amended) A method for fabricating a non-volatile memory device, the method comprising:

providing a semiconductor substrate;

forming a gate oxide layer on the substrate, the oxide layer having a noncrystalline structure;

forming a MgO layer overlying on the oxide layer after forming the oxide layer on the substrate, the MgO layer having a crystal structure;

thermally annealing the second buffer layer-MgO layer to enhance an alignment of crystallites of the second buffer MgO layer;

forming a ferroelectric material overlying the substrate and the MgO layer;
forming a gate layer overlying the ferroelectric material, the gate layer overlying a channel region; and

forming first and second doped regions adjacent to first and second ends of the channel region. wherein the gate oxide layer is a first buffer layer and the MgO layer is a second buffer layer.

- 22. Canceled.
- 23. (Original) The method of claim 21, wherein the oxide layer has an amorphous structure and the MgO layer has a crystal structure.
- 24. (Original) The method of claim 23, wherein the second buffer layer has a thickness of no more than 10 nm.
  - 25. (canceled)
- 26. (Original) The method of claim 21 wherein the second buffer layer is thermally annealed at a temperature of 800-1000 degrees Celsius.
- 27. (Previously Presented) The method of claim 21, wherein the MgO layer formed on the oxide layer is provided with a highly-oriented structure prior to the annealing step.
- 28. (Previously Presented) The method of claim 27, wherein the MgO layer has a polycrystalline structure prior to the annealing step.
- 29. (Currently Amended) A method for fabricating a non-volatile memory device, the method comprising:

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forming an oxide layer on the substrate, the oxide layer having a non-crystalline structure;

forming a MgO layer on the oxide layer, the MgO layer formed on the oxide layer having a highly-oriented structure;

forming a ferroelectric material overlying the substrate and on the MgO layer;
forming a gate layer overlying the ferroelectric material, the gate layer overlying a channel region; and

forming first and second doped regions adjacent to first and second ends of the channel region.

- 30. (Previously Presented) The method of claim 29, further comprising: thermally annealing the highly-oriented MgO layer to enhance an alignment of crystallites of the of the MgO layer.
- 31. (Previously Presented) The method of claim 29, wherein the MgO layer is formed after the oxide layer is formed on the substrate.
- 32. (Previously Presented) A method for fabricating a non-volatile memory device, the method comprising:

providing a semiconductor substrate;

forming an amorphous gate dielectric layer on the substrate;

forming a MgO layer on the amorphous dielectric layer after forming the dielectric layer on the substrate, the MgO layer having a highly-oriented structure; and

forming a ferroelectric layer overlying the MgO layer,

wherein the dielectric layer, MgO layer and ferroelectric layer are patterned to form a transistor.

- 33. (Previously Presented) The method of claim 32, wherein the MgO layer has a crystalline structure.
- 34. (Previously Presented) The method of claim 33, wherein the MgO has a polycrystalline structure.